Analysis of SRAM Memories

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Abstract: Area reduction and leakage current reduction are among the major area of concern in today's CMOS Technology. SRAM is a most common embedded memory for CMOS ICs and it uses bistable latching circuitry to store a bit. This paper provides comparative analysis on performance of different SRAM cells - 6T,8T and 12 T by considering layout, power and current values. The simulation output is obtained by using HSPICE tool.

Keywords: SRAM, CMOS, current, power, read, write.

I. Introduction

Memories are of two types Static Random Access Memory (SRAM) and Dynamic Random Access Memory (DRAM). SRAM is classified as a volatile memory because it depends upon the application of continuous power to maintain the stored data. The basic structure of SRAM has cross coupled inverter which hold the data which is stored. DRAM use charge storage on a capacitor to represent binary data values. The cells must be read and refresh at periodic intervals. It has high density.

SRAM densities is lagging behind DRAM mainly because of greater no of transistors. In SRAM more space is required than DRAM. For example a 1K memory will need 1K cells with each cell having 6 transistors. But for DRAM of 1K memory, it needs 1K cells and 1K capacitors. But DRAM needs periodic refresh with respect to capacitor which consumes more power. So SRAM is mostly used. The most popular among SRAM devices is the 6 transistor configuration. It has high speed and data stored in inverter connected back to back in which one inverter charges and other discharges [1].

SRAM cells have been the predominant technologies used to implement memory cells in computer systems [2]. SRAM cells are faster and require no refresh since reads are not destructive. Here SRAM cell built from a simple static latch and tri state inverter. The reading action itself refreshes the content of memory. The SRAM access path is split into two portions: from address input to word line rise and from word line rise to data output. The decoder which constitutes the path from address input to the word line rise is implemented as a binary structure by implementing a multi-stage path. For nearly 40 years CMOS memories have been scaled down in order to achieve higher speed, performance and lower power consumption. Due to their higher speed

SRAM based Cache memories and System-on-Chips are commonly used.

II. SRAM Structure

A. 6T SRAM Cell

A SRAM cell must be designed in such a way to provide proper read operation and reliable write operation. In the conventional 6T SRAM cell this is fulfilled by appropriately sizing all the transistors in the SRAM cell [3]. It has symmetrical structure. The structure of 6T SRAM is shown in figure 1.

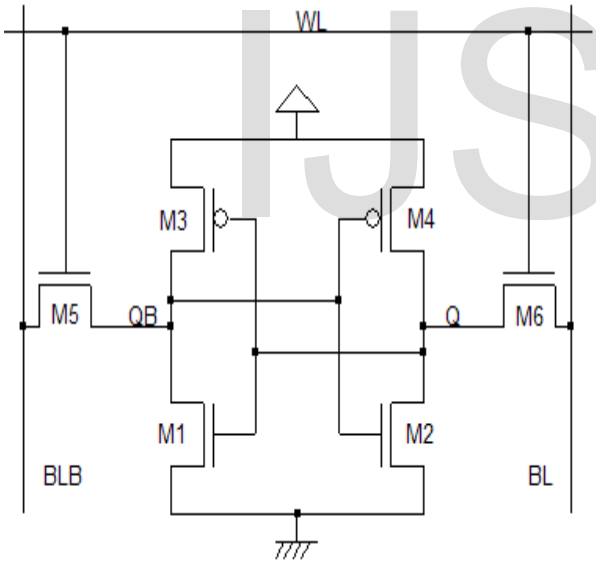

Figure 1 : Structure of 6T SRAM

In this circuit, storage nodes are specified by QB, Q. Suppose that node QB stores “0” then node Q stores “1. In this case, M1, M4 are turned on. Also, M2 and M3 are turned off. During the hold time, when Word Line (WL) is not selected (idle mode), M5and M6 are turned off. In idle mode, M5 and M2 give a small rise on node X because of leakage currents. When data ‘1’ to be written in the cell the Bit Line (BL) is made ‘1’ and Word Line (WL) is made ‘1’ and data is stored in the cross coupled inverter which can read when required [4]. In 6T SRAM read noise margin is less

B. 8T SRAM Cell

8T SRAM cell is not symmetrical in structure when compared to 6T SRAM cell. The structure is given in figure 2. The 8T cell has a separate read port comprised of transistor M5 [5]. This structure of 8T cell enables stable red operation without sizing of the additional transistors and the driver transistor at the read port and the drive transistors. Write time is high and area is more. Due to unsymmetrical structure fabrication of the device is difficult when compared to 6T cell though it offers fast recovery of data [6].

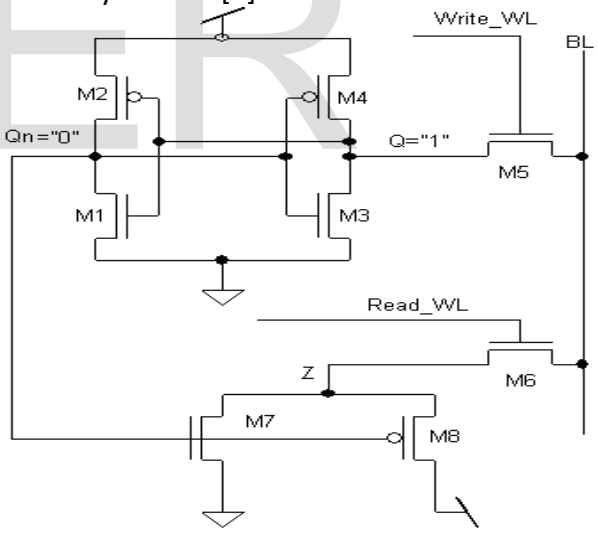

Figure 2 : Structure of 8T SRAM

C. 12T SRAM Cell

The structure of 12 T SRAM in shown in figure 3 which has pass transistor and inverter. It also contains precharge circuit which serves to charge the Bit Line (BL) and Bit Line Bar (BLB) to VDD. The Precharge (PC) signal enables the bit-lines

to be pre-charged at all times except during write and read cycle [7]. The transistor M1 and M2 will precharge the bitlines while the transistor M3 will equalize them to ensure both bit lines within a pair are at the same potential before the cell is read.

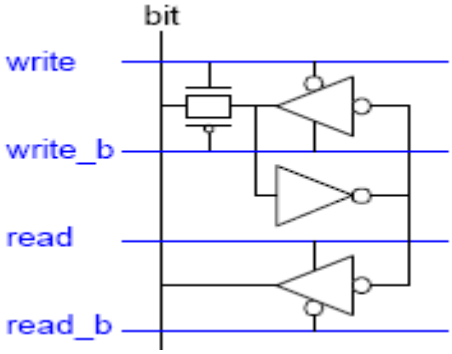

Figure 3: Structure of 12 T SRAM

III. Simulation Results

The simulation result obtained from HSPICE tool with respect to write and read operation of 6T. 8T and 12T SRAM is given below [8]. Comparison is made based on various parameters also shown below [9].

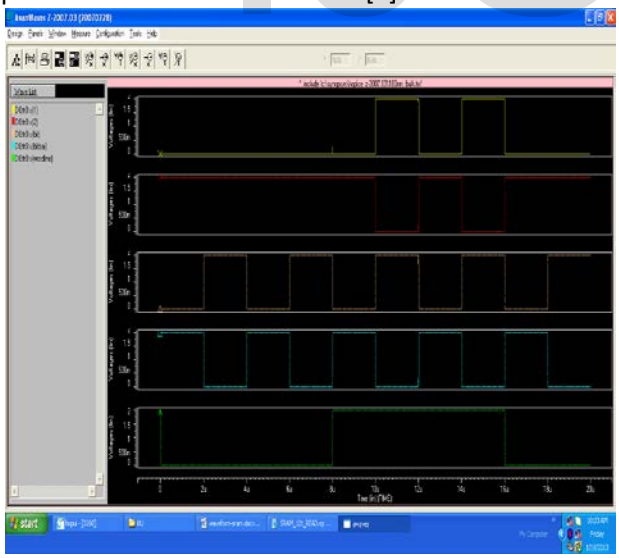

Figure 4 : WRITE Operation - 6T SRAM

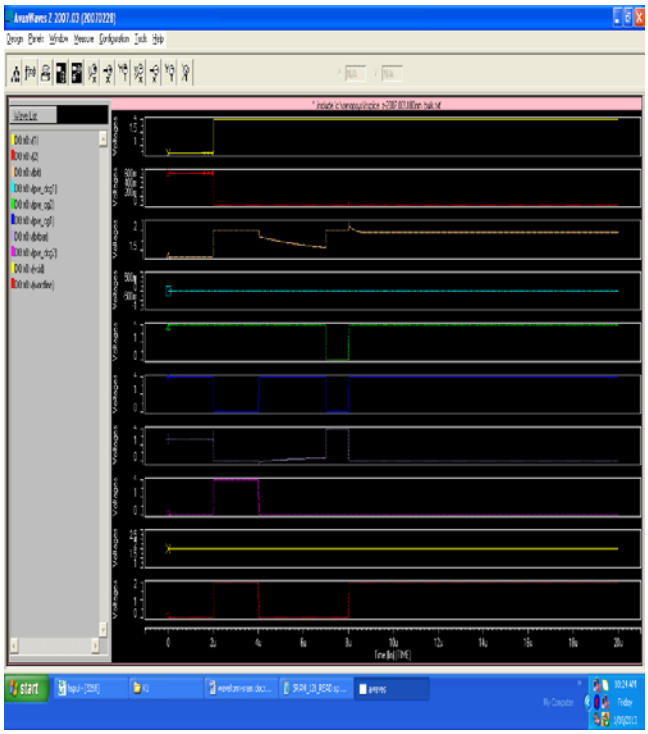

Figure 5: READ Operation - 6T SRAM

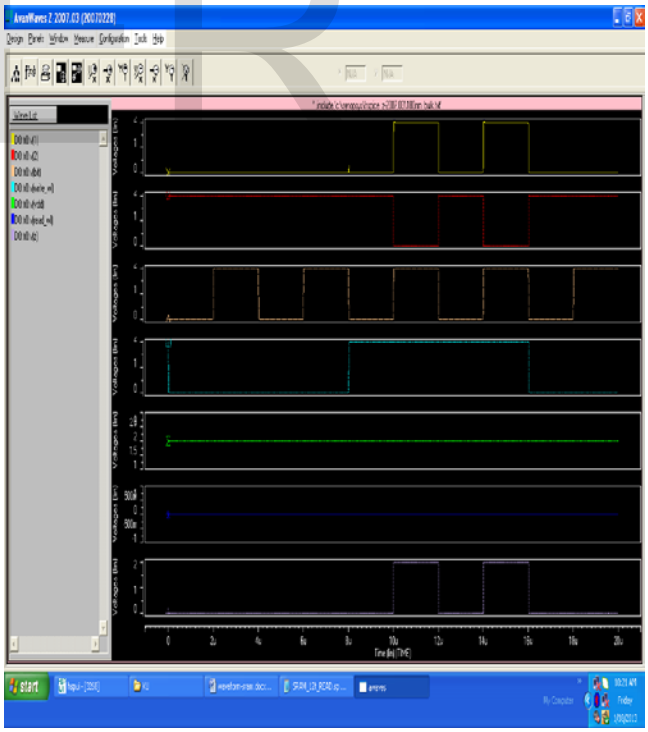

Figure 6 : WRITE Operation - 8T SRAM

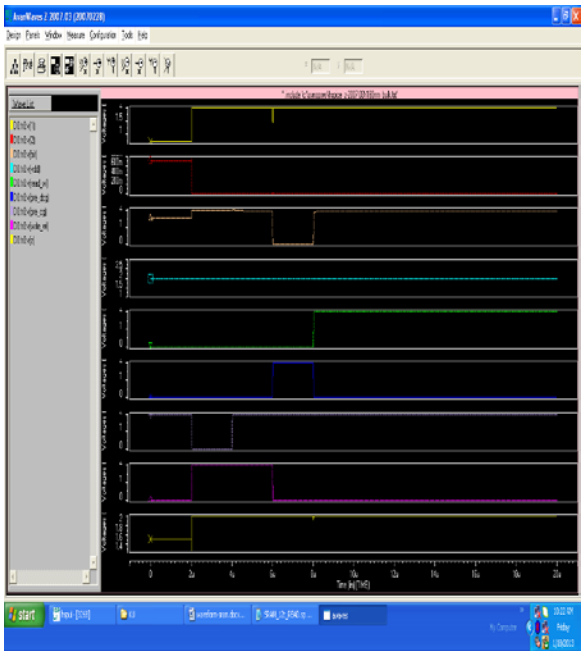

Figure 7 : READ Operation - 8T SRAM

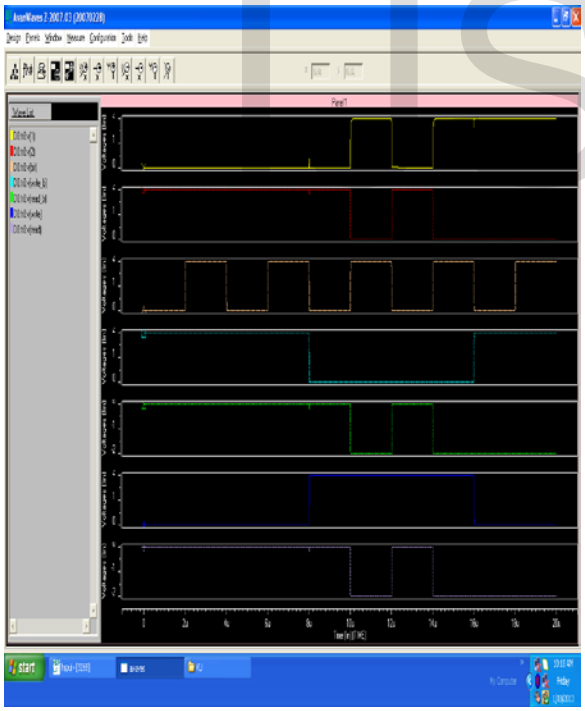

Figure 8 : WRITE Operation - 12T SRAM

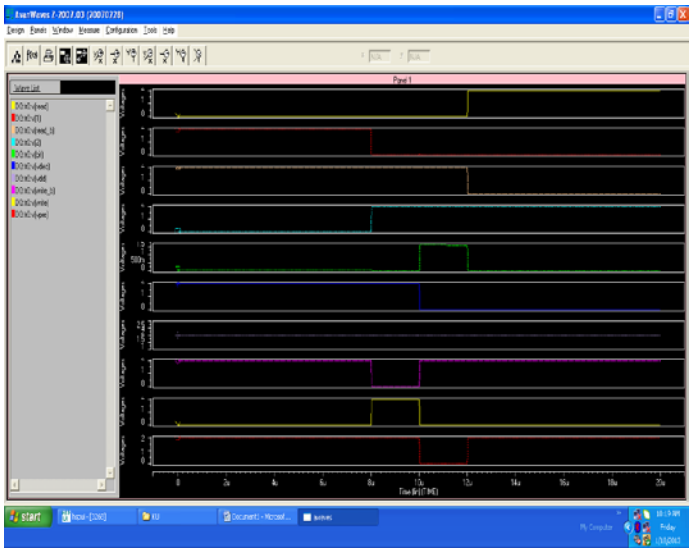

Figure 9 : READ Operation - 12T SRAM

The comparison between the transistor based on current and power during read and write operations are given in table 1

Table 1: Comparison of 6T,8T and 12 T SRAM

S:no	Types of SRAM	Write		Read	
		Current (max)	Power (max)	Current (max)	Power (max)
1	6T	400µA	60µw	500nA	100µW
2	8T	400µA	55µw	400nA	60µW
3	12T	200nA	5mw	500nA	1mW

By comparing the parameters the value of current decreases or remains constant with respect to 6T, 8T and 12T cells during write and read operation but power value increases in 12T when compared to 6T and 8T since area increases in 12T . But the capability to hold the data using 12T is high which can be observed in the simulation result of 12T write and read operation. So by increasing the number of transistors the area increases and hence power increases. The capability to hold the data in presence of noise can be obtained by increasing the number of transistors.

IV Conclusion

The different configurations of SRAM transistor have been simulated by performing write and read operation and compared. The 6T SRAM provide very less read noise margin which is further degraded due to process variation. The 8T SRAM cell provide higher read noise margin but its write noise margin is very small. Hence it is more prone to failure during write operation. In 12T SRAM the power value is high but it is efficient in holding the data. But increase in area causes increase in power consumption and increase in cost.

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